
Viterbi Decoder 1.1 – Data sheet

1. Introduction

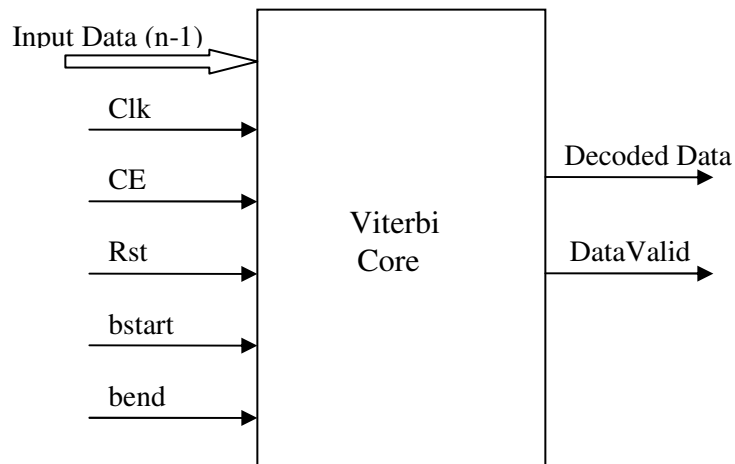
Tetcos's Viterbi Decoder is a parameterizable high performance IP core that performs decoding of the convolutionally encoded data. This core supports various code rates, constraint lengths and operates in continuous and block mode. The core offers designers a standard compliant platform to accelerate development process and reduce time to market.

2. Features

- Code rates : $1/n$, where $n = 2, 3, 4, 5, 6$.
- Parameterizable constraint length (L) from 3 to 8.
- Parameterizable trace back length: $3 \times \text{Constraint Length (3L)}$ to $14 \times \text{Constraint Length (14L)}$.
- Operates in continuous and block mode
- Supports Zero flushing block decoding method
- Accepts Hard Decision and Soft decision data inputs
- Parameterizable Soft decision data width
- Offset-binary and signed magnitude soft data representation
- Latency: $[4 \times \text{Trace back length}] + 8$ clock cycles for continuous decoding.
- Provides standard interface with external devices.
- Standard Generator polynomials as given in the table below.

Rate	Constraint Length	Vectors (in Octal)	
1/2	3	5,7	
	4	15,17	
	5	23,35	
	6	53,75	
	7	133,171	
	8	247,371	
	1/3	3	5,7,7
		4	13,15,17
5		25,33,37	
6		47,53,75	
7		133,145,175	
8		225,331,367	
1/4		3	5,7,7,7
		4	13,15,15,17
	5	25,27,33,37	
	6	53,67,71,75	
	7	133,135,147,163	
	8	235,275,313,357	
	1/5	3	7,7,7,5,5
		4	17,17,13,15,15
5		37,27,33,25,35	
6		75,71,73,65,57	
7		175,131,135,135,147	
8		257,233,323,271,357	
1/6		3	7,7,7,7,5,5
		4	17,17,13,13,15,15
	5	37,35,27,33,25,35	
	6	73,75,55,65,47,57	
	7	173,151,135,135,163,137	
	8	253,375,331,235,313,357	

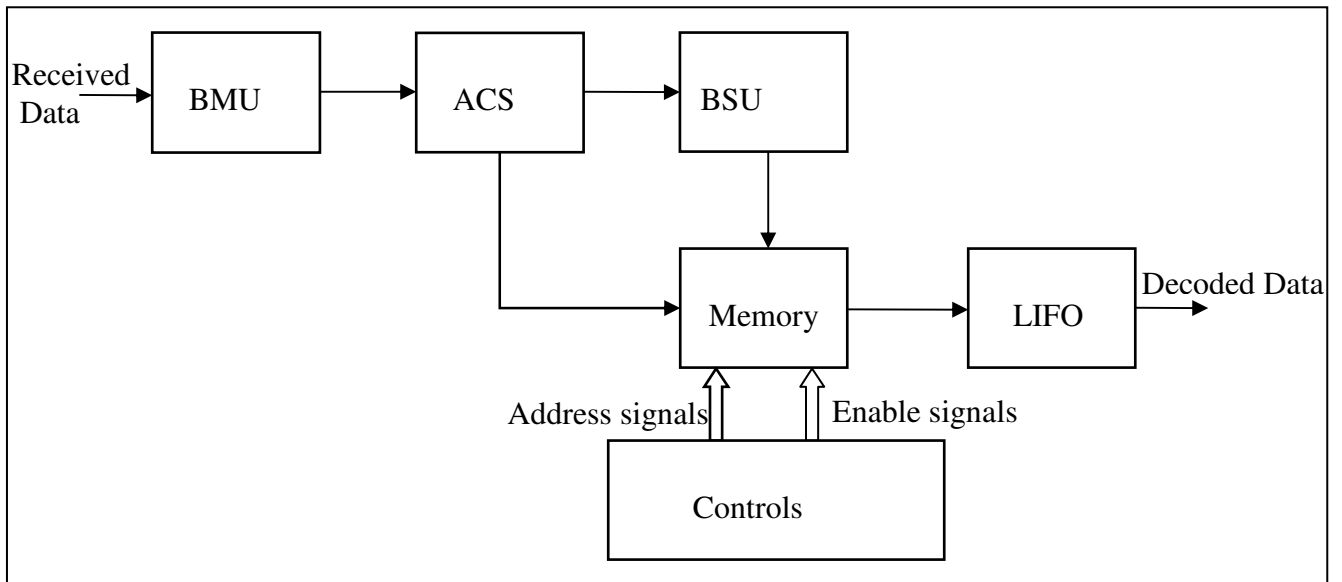
3. Core Pin-Outs



4. Signal Description

Signal Name	Direction	Size	Description
Clk	Input	1 bit	Clock signal input pin
Rst	Input	1 bit	Reset pin
Din	Input	(n-1 Downto 0) Where n is the number of output bits from encoder	Input data to Viterbi decoder. Each Din signal of width n for soft decision data width of n and 1 for hard decision
CE	Input	1 bit	Chip select pin. Decoder is active in continuous mode only when CE is high.
bstart	Input	1 bit	Indicates the start of the block of data (Block Mode)
bend	Input	1 bit	Indicates the end of the block of data (Block Mode)
DataValid	Output	1 bit	Indicates the presence of data at output pin.
Decoded data	Output	1 bit	Decoded output data

5. Block Diagram



5.1. Description of the block diagram

Branch Metrics Unit (BMU):

This unit is used to find the branch metrics of each transition occurs on the trellis diagram.

Add-Compare-Select Unit (ACS):

This unit is used to calculate the path metrics of each transition on trellis tree and select the surviving state with least path metrics by comparing the two path metrics. Finally the updated path metrics of each state is stored in the path metrics table.

Best State Unit (BSU):

BSU finds the best state (state with the least path metrics value) for every data bits received. Best state is used to initiate the trace-back algorithm in memory.

Memory:

States selected by the ACS unit needs to be updated in the memory for decoding the original data by trace-back algorithm. BRAM is used to store the state information and the size of memory varies with respect to trace-back length. Trace-back algorithm is implemented in memory unit.

Controls:

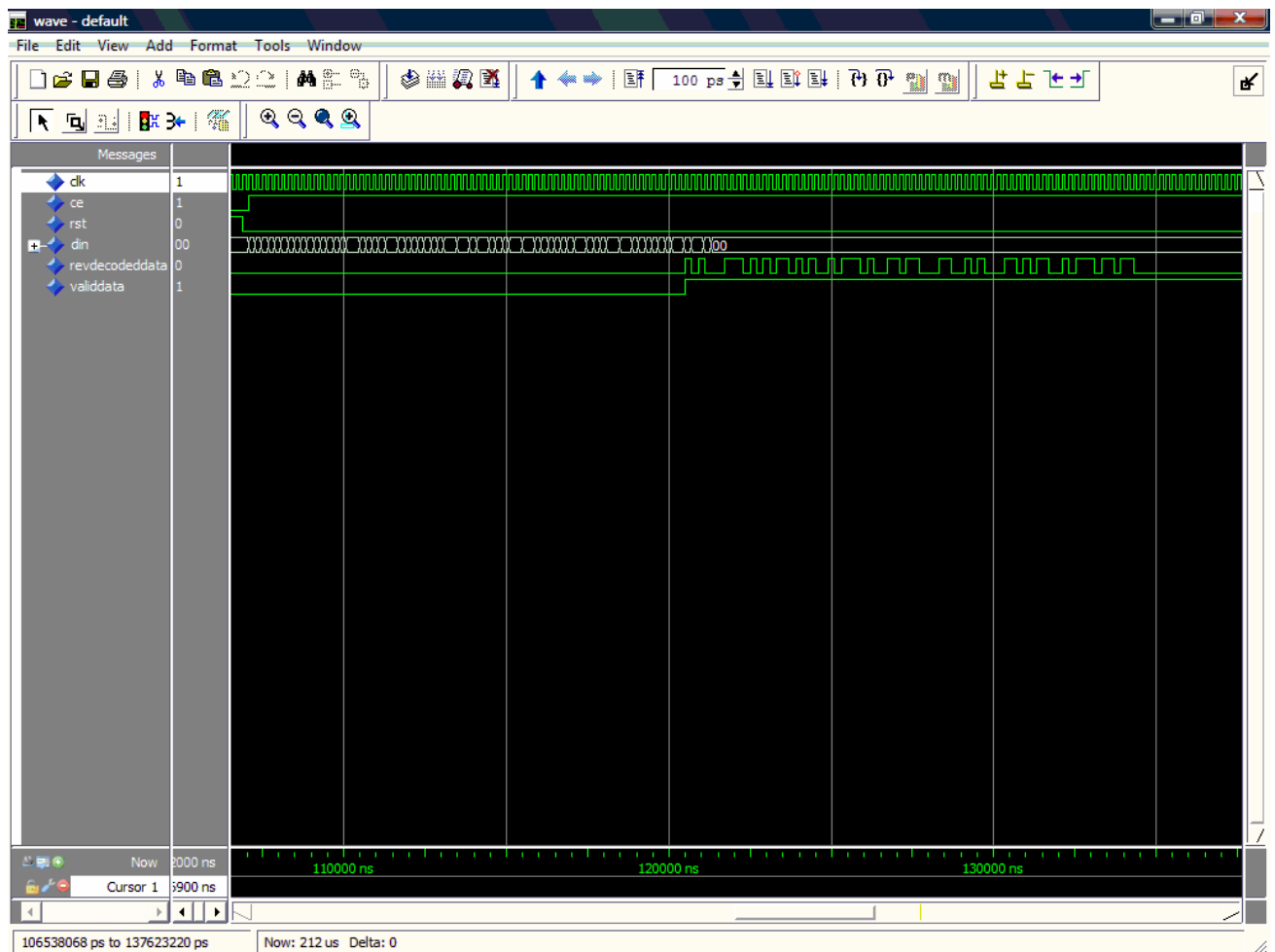
Controls unit generates the necessary control signals to access memory. It generates the signals like read address, write address, read enable and write enable.

Last-In-First-Out Register (LIFO):

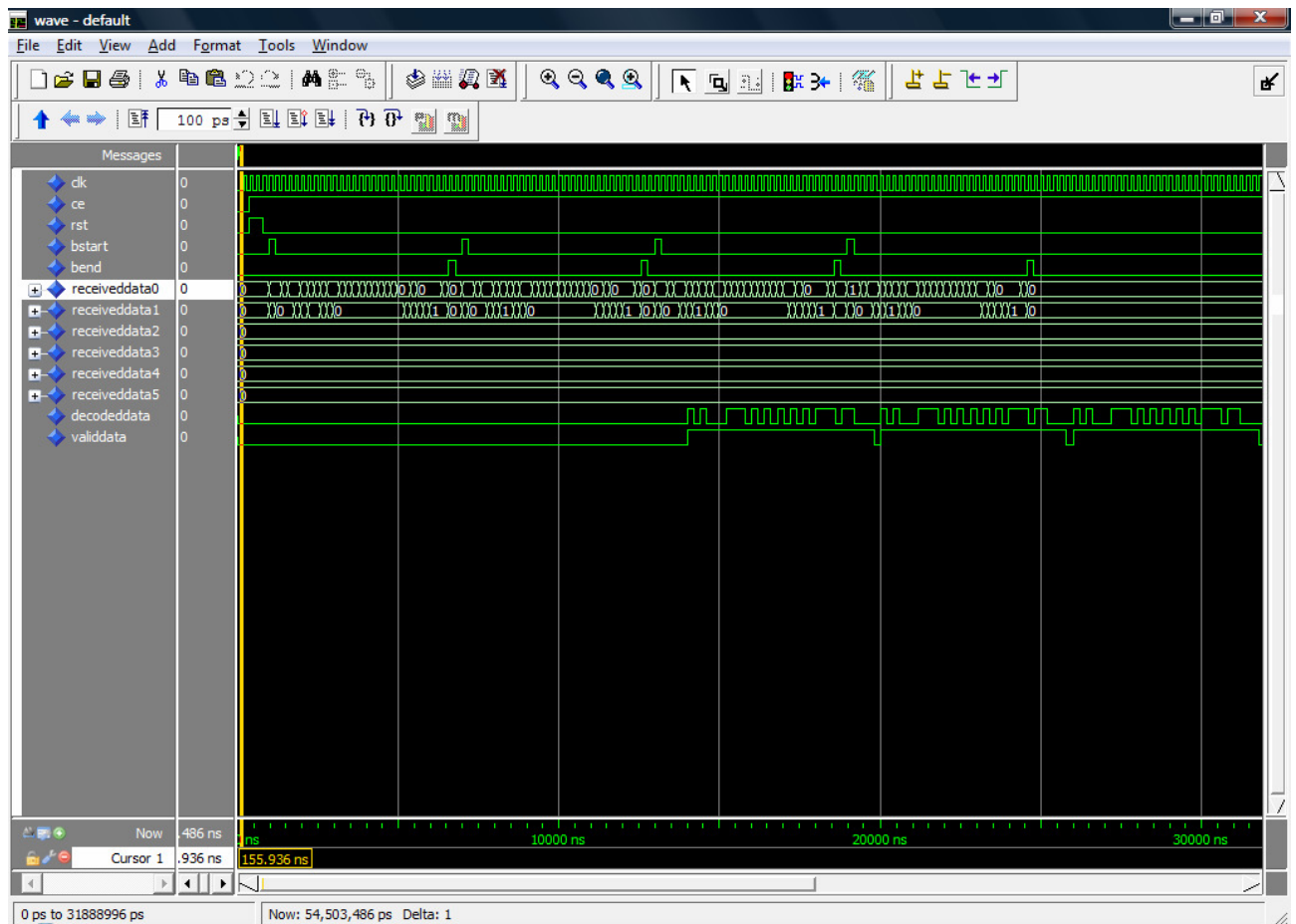
Trace-back data from memory will be in the reverse order. This reverse-data is given to LIFO for correct ordering. Output of this module is the decoded data.

6. Timing diagram (Simulation Snapshot)

TD-01.Continuous Viterbi Decoding



TD-02.Block Viterbi Decoding



7. Performance Metrics

For Constraint length=7, Rate=1/2 and Trace-back length=96

Device	XC3S500E (Spartan3E)	XC5VLX50T (Virtex 5)
Slices	2073	1701
LUT-FF Pairs	Not Applicable	1575
FFs	1397	1940
LUTs	3637	4864
BRAMs	4	2
Maximum Frequency	48.942 MHz	142.382 MHz

8. Deliverables

- Fully Synthesizable VHDL code / Technology Specific Netlist
- Fully Functional Test bench
- Detailed User Guide

9. Services and Support



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